Things I learned while designing the Epiphany & Parallella

Presentation at Chalmers University of Technology
Feb 2, 2015
Adapteva Overview:

- Semiconductor company founded in 2008
- 64-core 28nm processor achieves 50 GFLOPS/W
- $900K “Parallella” Kickstarter funding 2012
- $3.6M Series-B in 2013 (Ericsson)
- 10,000 customers and $2M revenue in 2014
The Epiphany Multicore Architecture

- ANSI-C, OpenCL, MPI, OpenMP
- Scalable to “infinity” (4096 cores/chip at 28nm)
- Distributed memory model
- 50 GFLOPS/W (25mW & 0.13mm$^2$ per core)
About Me: Before Adapteva

8 years designing DSPs
100 people, $100M R&D
TigerSHARC was a tech success, but a huge financial flop!

Mixed signal SOCs for CCDs
Invented new ISA in 2 weeks
3-4 designers per derivative
Huge success (> $100M)
For DSP it's much more efficient to design a pipeline of specialized processors than having a single massive processor that runs a complete application.
Goals for Epiphany (2008)

- Floating point (industrial + medical markets)
- ANSI-C programmable
- Scalable
- 10X boost in GFLOPS/Watt (otherwise, who would buy?)
- Realizable by a team < 5 engineers
Old Architecture Process
(Waterfall model)

1) Application/system engineer creates a strawman
2) Performance tested in simulation
3) Microarchitecture development
4) RTL development
5) Synthesis and place and route
6) Build chips, wait for feedback, go back to “1” (12-24 months)

Still the norm today to have different people for each task and not to feedback information to previous step. (successful SOC companies are smarter than this)
My Architecture Process

- One person owns the whole path from arch to layout
- Spreadsheet (triangulating architectures)
- Emacs (does code look clean on paper?)
- Manually “count” gates in code. “Feel complexity”
- Verilog Simulation (checks for logical/mental mistakes)
- Synthesize design (in FPGA or EDA to measure cost!!)
- Use advisors (peer review to look for gotchas)
- Application development (No but I should have!!) (*considering the lack of benchmarks, it's a small miracle Epiphany works as well as it does)
Step 1: Study History

My inspiration of what to do (and NOT to do)

- Henessy and Patterson's classic books. (Re)Read them!
- Blackfin, TigerSHARC, and c64x (DSP features)
- ARM and MIPS (standard features)
- Tilera and Ambric (manycore features)

My rule: Watch out for “clever” features! The really useful features will be common to all archs in a class.
Step 2: Create a baseline

- How much area goes to computation?
- How expensive is a floating point unit?
- How expensive is SRAM and cache?
- How expensive is the Network?
- What is the performance gain of instruction X?
- How often is instruction X used?
- What does a typical program look like?

These numbers are your anchor, get them right!
Step 3: Verify assumptions

- Design and simulate (to verify cost assumptions)
- Build prototypes (to verify simulation assumptions)
- Talk to customers (to verify application and product feature assumptions)
## Summary of Choices

<table>
<thead>
<tr>
<th>Dilemma</th>
<th>Choice</th>
<th>Reason</th>
<th>Outcome</th>
</tr>
</thead>
<tbody>
<tr>
<td>Programming Lang</td>
<td>C</td>
<td>No brainer</td>
<td>Great (common)</td>
</tr>
<tr>
<td>Memory size</td>
<td>32KB</td>
<td>Tapeout cost</td>
<td>Poor (needed 64KB)</td>
</tr>
<tr>
<td>Load-stores</td>
<td>64-bit single LD/ST</td>
<td>Compromise</td>
<td>Great</td>
</tr>
<tr>
<td># Memory banks</td>
<td>4</td>
<td>Compromise</td>
<td>Great</td>
</tr>
<tr>
<td># Registers</td>
<td>64</td>
<td>Compromise</td>
<td>Great</td>
</tr>
<tr>
<td>2\textsuperscript{nd} Integer Instr?</td>
<td>Yes</td>
<td>Hedge</td>
<td>Great (see bcrypt..)</td>
</tr>
<tr>
<td>NOC flits</td>
<td>Yes</td>
<td>Efficiency</td>
<td>Great</td>
</tr>
<tr>
<td>NOC buffers</td>
<td>Yes</td>
<td>Efficiency</td>
<td>Great</td>
</tr>
<tr>
<td>Byte addressing</td>
<td>Yes</td>
<td>General purpose</td>
<td>Great</td>
</tr>
<tr>
<td>Debug, interrupts</td>
<td>Yes</td>
<td>General purpose</td>
<td>Great</td>
</tr>
<tr>
<td>Hardware caching</td>
<td>No</td>
<td>Power</td>
<td>Great</td>
</tr>
</tbody>
</table>
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<tbody>
<tr>
<td>No special instr</td>
<td>No</td>
<td>Efficiency</td>
<td>50 GFLOPS/W</td>
</tr>
<tr>
<td>64bit floating point</td>
<td>No</td>
<td>overkill</td>
<td>Didn't matter</td>
</tr>
<tr>
<td>Branch target buffer</td>
<td>No</td>
<td>power</td>
<td>Great</td>
</tr>
<tr>
<td>Push/pop</td>
<td>No</td>
<td>Limit function calls</td>
<td>Good enough</td>
</tr>
<tr>
<td>Dual issue</td>
<td>Yes</td>
<td>2x perf (!2x power)</td>
<td>Great</td>
</tr>
<tr>
<td>Stall scoreboard</td>
<td>Yes</td>
<td>Ease of use</td>
<td>Great</td>
</tr>
<tr>
<td>LVDS</td>
<td>Yes</td>
<td>Performance</td>
<td>Great</td>
</tr>
<tr>
<td>PLL on chip</td>
<td>No</td>
<td>No $$</td>
<td>Great</td>
</tr>
<tr>
<td>SERDES</td>
<td>No</td>
<td>No $$</td>
<td>Great</td>
</tr>
<tr>
<td>Integer multiply</td>
<td>No</td>
<td>Power</td>
<td>Poor (very common)</td>
</tr>
</tbody>
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</tr>
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<tbody>
<tr>
<td>Signed byte load</td>
<td>No</td>
<td>power</td>
<td>Not good (limits apps)</td>
</tr>
<tr>
<td>Streaming IO protocol</td>
<td>Autoburst</td>
<td>Simplicity/latency</td>
<td>OK (random only at 25% peak)</td>
</tr>
<tr>
<td>Pipeline depth</td>
<td>5+3</td>
<td>Compromise</td>
<td>Great</td>
</tr>
<tr>
<td>Autoincrement LDR</td>
<td>Yes</td>
<td>Efficiency</td>
<td>OK (no compiler support)</td>
</tr>
<tr>
<td>Hardware loops</td>
<td>Yes</td>
<td>Benchmarks</td>
<td>OK (no compiler support)</td>
</tr>
</tbody>
</table>
Some Hardware Lessons

- Architects should be vertically integrated
- Tiled architectures are MAGICAL
- Symmetry is a very powerful design principle with sometimes unexpected rewards
- Designing leading edge chips is fairly easy today for a small team with the right experience (<<$100M)
- Designing boards is easier than designing chips but not trivial
- Never push the tools, process, or capabilities of your vendor (they will break).
Some Software Lessons

- Modern compilers are incredible (given enough registers and a small instruction set)
- Customers take the path of least resistance
- Developers take the path of least resistance
- Surprisingly hard to find applications that need more performance....
  ...and those applications are really complex..
  ..meaning they have tons of legacy stack software...
- SW trumps energy efficiency in 99.99% of applications
Epiphany (-1)

- May 2008
- Naive but close...
- Could have had 64 cores in 2008!
- Epiphany arch has only changed by “delta” since 2008
- Submitted many grant proposals (all rejected)
Epiphany-0

- Oct 2008 synthesis and layout prototype
- Virtual prototypes (synthesis and layout of cores)
- Showed that 1 Ghz operation and 50GFLOPS/W was possible
- Gave me the courage to ask F&F for money ($200K seed)
Epiphany-I

- Jun 2009 tapeout
- 16 cores, 65nm prototype
- ~1 person, 12 weeks
- Changes same day as TO!
- Barely worked but proved it was possible
- ~12mm^2
Lesson: Team makeup is the #1 determinant for success. You must have it in place before you set out on journey.
Epiphany-II

- May 2010 tapeout
- 16 cores, 65nm
- ~3 person, ~6 weeks
- Changes 1 day before TO
- A vendor screwed up (lucky for us...)
- Should have been a product
- ~12mm^2
It Works!

- Sept 2010 bringup
- Ran floating point program!
- Provided efficiency!
- Packaging yield was less than 10% on eLink (vendor).
- SPI backdoor was key to debugging vendor packaging issue
Epiphany-III

- Dec 2010 tapeout
- 16 cores, 65nm
- This is a product!
- Kept improving with every iteration
- RTL changes 1 day before TO
- ~25 GFLOPS/W
- ~12mm^2
New Packaging

- 60um staggered pitch is not trivial!
- Vendor failure on E-1 and E-2 almost broke company!
- New vendor (Kyocera)
- You can't be on the bleeding edge without the right partners!
- Better results!
First Delivery

- May 2011
- Chip worked perfectly out of the box!
- This silicon became the E16G301
- Felt at peace
- Happy moment, but only the beginning...
ESC-SV 2011

- May, 2011
- Launched Epiphany-III
- Lots of press!
- Fun...
- But where were the customers!!???
Epiphany-IV

- Aug 2011 tapeout
- (Jul 2012 samples)
- 64 cores, 28nm
- 50 GFLOPS/W
- RTL changes 2 days before TO
- Done in 12 weeks!
More HW...

- Feb 2012 IP demo
- IP demo of 1024 cores
- IP demo of DPF
- IP demo of 128KB SRAM
- 1 day to layout each
First Product

- May, 2012 ship
- FMC board from Bittware
- 4 chips in array
- Not cheap!
- Never shipped in volume
Software

- 2012 focus
- Invested heavily in software tools + demos
- Face recognition, FFT, Matmul
- Beat ARM by 10X on demo for BIG smartphone company!
- Response: “Meh...”
Parallella

• Sept, 2012
• We needed a parallel community and a better kit, so the $99 Parallella was born, Sept 2012
• KS combines pre-purchase, community, and marketing.
OPTIMISTIC & STUBBORN

Project Funding Successful

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Success?

- Nov 2012
- Woke up next morning stressed and behind schedule.
- Only sell what you have!!
Powerup (Gen0)

• May 2013
• My first board and it worked!
• Only minor issues
• Challenge was super aggressive design targets (credit card, features, cost, schedule)
Gen0 Release

- July 2013
- Gen0 board released!
- We build working cluster with 42 boards!
- Sent out 50 boards to KS backers, only ~1 (NOTZED) got significant use!
Chips are back!

- Aug 2013
- Full mask
- New Tier-1 package vendor (ASE).
  Awesome company!
- 90% yield!
- Good thermals
- 100/100 grade
- Now we need to test 10,000 chips!?
New Investment

- Dec 2013 closing
- $3.6M from Ericsson + VC
- Published WP showing 25X edge over Intel
- Great...but we were still buried in KS commitments and logistics issues...
2014 Distractions: T-shirts, cases, logistics, accessories... (sourcing industrial design is not us!) What is Adapteva again?
More HW...

- June 2014
- Shipped to 200 Universities & 10,000 developers
- Built the “A1”, the world's densest cluster.
- Where are the BIG customers??
MY FINAL LESSON:
(took me 7 years to learn)

IT'S THE SOFTWARE
STUPID!!!!
..but we are still going!!

The Parallel Architectures Library

- Compact C library with optimized routines for vector math, synchronization, and multi-processor communication.
- Designed for parallel and memory constrained hardware
- Designed to be portable across multiple ISAs
- Open source (apache 2.0 permissive license)
- Open invitation to participate!!
- https://github.com/parallella/pal

NEW!
What I (still) Know:

- Moore's law WILL come to an end
- Parallel computing is inevitable
- Architectures like Epiphany are the future
- CPUs, FPGAs, and manycore will coexist
- The world will continue to be driven by $$42$$